What is claimed is:

1. A receiver circuit comprising:

a sampling circuit sampling an input signal;

a buffer circuit buffering an output of said sampling circuit;

a determining circuit determining an output of said buffer circuit; and

a buffer control circuit keeping a small input signal dependency of the output of said buffer circuit until carrying out said sampling.

2. The receiver circuit as claimed in claim 1, wherein said buffer control circuit is a switch arranged between said buffer circuit and a power line.

3. The receiver circuit as claimed in claim 1, wherein said buffer control circuit is a switch arranged between the output of said buffer circuit and a load device.

4. The receiver circuit as claimed in claim 1, further comprising a precharge circuit precharging an input of said determining circuit before said sampling circuit samples the input signal.

5. The receiver circuit as claimed in claim 1, wherein said sampling circuit comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

6. The receiver circuit as claimed in claim 1, wherein said buffer circuit comprises a plurality of buffer circuit units, and characteristics of a signal transmission path is compensated by adjusting a magnitude of an output of said buffer circuit units.

7. The receiver circuit as claimed in claim 1, wherein said buffer circuit is a transconductor converting an input voltage to a current, and said buffer control circuit is a current source switch which keeps a small current of said transconductor until carrying out

said sampling.

8. The receiver circuit as claimed in claim 1, wherein said buffer circuit comprises a micro current circuit for keeping a micro current flowing in said buffer circuit before said sampling circuit samples the input signal.

9. The receiver circuit as claimed in claim 1, further comprising a switching circuit, ensuring a substantially constant output of said buffer circuit when said sampling circuit samples the input signal, provided at the output of said buffer circuit.

10. A receiver circuit comprising:

a sampling circuit sampling an input signal;

a buffer circuit buffering an output of said sampling circuit;

a determining circuit determining an output of said buffer circuit; and

a buffer control circuit keeping a substantially constant value of the output of said buffer circuit until carrying out said sampling.

11. The receiver circuit as claimed in claim 10, wherein said buffer control circuit is a switch arranged between said buffer circuit and a power line.

12. The receiver circuit as claimed in claim 10, wherein said buffer control circuit is a switch arranged between the output of said buffer circuit and a load device.

13. The receiver circuit as claimed in claim 10, further comprising a precharge circuit precharging an input of said determining circuit before said sampling circuit samples the input signal.

14. The receiver circuit as claimed in claim 10, wherein said sampling circuit comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

15. The receiver circuit as claimed in claim 10, wherein said buffer circuit comprises a plurality of buffer circuit units, and characteristics of a signal transmission path is compensated by adjusting a magnitude of an output of said buffer circuit units.

16. The receiver circuit as claimed in claim 10, wherein said buffer circuit is a transconductor converting an input voltage to a current, and said buffer control circuit is a current source switch which keeps a small current of said transconductor until carrying out said sampling.

17. The receiver circuit as claimed in claim 10, wherein said buffer circuit comprises a micro current circuit for keeping a micro current flowing in said buffer circuit before said sampling circuit samples the input signal.

18. The receiver circuit as claimed in claim 10, further comprising a switching circuit, ensuring a substantially constant output of said buffer circuit when said sampling circuit samples the input signal, provided at the output of said buffer circuit.

19. A receiver circuit comprising:

a sampling circuit sampling an input signal;

a determining circuit determining an output of said sampling circuit; and

a sampling control circuit dynamically changing a transconductance from the input to the output of said sampling circuit and sufficiently reducing the input signal dependency of the output of said sampling circuit at other than a sampling time point.

20. The receiver circuit as claimed in claim 19, wherein said sampling control circuit changes by switching the transconductance from the input to the output of said sampling circuit.

21. The receiver circuit as claimed in claim 20, wherein said transconductance is switched by switching a

tail current of a differential transistor pair.

22. The receiver circuit as claimed in claim 21, wherein said tail current is switched by switching a current path between a route of said tail current of said transconductor and the other routes.

23. The receiver circuit as claimed in claim 22, wherein said current is switched by a transistor switch for switching the drain current of said differential transistor pair.

24. The receiver circuit as claimed in claim 22, wherein said current is switched by injecting to a source of the input transistor of said transconductor a current in such a direction as to turn off said input transistor.

25. The receiver circuit as claimed in claim 22, wherein said current is switched by use of a transistor connected in parallel such that the period during which said tail current flows is determined by the superposed portion of multi-phase clock signals.

26. The receiver circuit as claimed in claim 22, wherein said current is switched by use of a transistor connected in series such that the period during which said tail current flows is determined by the superposed portion of multi-phase clock signals.

27. The receiver circuit as claimed in claim 22, wherein a plurality of said sampling circuits sample different bit cells for a single determining circuit, and a weighted sum of the outputs of a plurality of said sampling circuits is determined.

28. A signal transmission system comprising a driver circuit, a signal transmission portion and a receiver circuit receiving an output of said driver circuit sent through said signal transmission portion, wherein said receiver circuit comprises:

a sampling circuit sampling an input signal;

a buffer circuit buffering an output of said sampling circuit;

a determining circuit determining an output of said buffer circuit; and

a buffer control circuit keeping a small input signal dependency of the output of said buffer circuit until carrying out said sampling.

29. The signal transmission system as claimed in claim 28, wherein said buffer control circuit is a switch arranged between said buffer circuit and a power line.

30. The signal transmission system as claimed in claim 28, wherein said buffer control circuit is a switch arranged between the output of said buffer circuit and a load device.

31. The signal transmission system as claimed in claim 28, wherein said receiver circuit further comprises a precharge circuit precharging an input of said determining circuit before said sampling circuit samples the input signal.

32. The signal transmission system as claimed in claim 28, wherein said sampling circuit comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

33. The signal transmission system as claimed in claim 28, wherein said buffer circuit comprises a plurality of buffer circuit units, and characteristics of a signal transmission path is compensated by adjusting a magnitude of an output of said buffer circuit units.

34. The signal transmission system as claimed in claim 28, wherein said buffer circuit is a transconductor converting an input voltage to a current, and said buffer control circuit is a current source switch which keeps a small current of said transconductor until carrying out said sampling.

35. The signal transmission system as claimed in claim 28, wherein said buffer circuit comprises a micro current circuit for keeping a micro current flowing in said buffer circuit before said sampling circuit samples

the input signal.

36. The signal transmission system as claimed in claim 28, wherein said receiver circuit further comprises a switching circuit, ensuring a substantially constant output of said buffer circuit when said sampling circuit samples the input signal, provided at the output of said buffer circuit.

37. A signal transmission system comprising a driver circuit, a signal transmission portion and a receiver circuit receiving an output of said driver circuit sent through said signal transmission portion, wherein said receiver circuit comprises:

a sampling circuit sampling an input signal;

a buffer circuit buffering an output of said sampling circuit;

a determining circuit determining an output of said buffer circuit; and

a buffer control circuit keeping a substantially constant value of the output of said buffer circuit until carrying out said sampling.

38. The signal transmission system as claimed in claim 37, wherein said buffer control circuit is a switch arranged between said buffer circuit and a power line.

39. The signal transmission system as claimed in claim 37, wherein said buffer control circuit is a switch arranged between the output of said buffer circuit and a load device.

40. The signal transmission system as claimed in claim 37, wherein said receiver circuit further comprises a precharge circuit precharging an input of said determining circuit before said sampling circuit samples the input signal.

41. The signal transmission system as claimed in claim 37, wherein said sampling circuit comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to

said sample switches are provided.

42. The signal transmission system as claimed in claim 37, wherein said buffer circuit comprises a plurality of buffer circuit units, and characteristics of a signal transmission path is compensated by adjusting a magnitude of an output of said buffer circuit units.

43. The signal transmission system as claimed in claim 37, wherein said buffer circuit is a transconductor converting an input voltage to a current, and said buffer control circuit is a current source switch which keeps a small current of said transconductor until carrying out said sampling.

44. The signal transmission system as claimed in claim 37, wherein said buffer circuit comprises a micro current circuit for keeping a micro current flowing in said buffer circuit before said sampling circuit samples the input signal.

45. The signal transmission system as claimed in claim 37, wherein said receiver circuit further comprises a switching circuit, ensuring a substantially constant output of said buffer circuit when said sampling circuit samples the input signal, provided at the output of said buffer circuit.

46. A signal transmission system comprising a driver circuit, a signal transmission portion and a receiver circuit receiving an output of said driver circuit sent through said signal transmission portion, wherein said receiver circuit comprises:

a sampling circuit sampling an input signal;

a determining circuit determining an output of said sampling circuit; and

a sampling control circuit dynamically changing a transconductance from the input to the output of said sampling circuit and sufficiently reducing the input signal dependency of the output of said sampling circuit at other than a sampling time point.

47. The signal transmission system as claimed in claim 46, wherein said sampling control circuit changes by switching the transconductance from the input to the output of said sampling circuit.

48. The signal transmission system as claimed in claim 47, wherein said transconductance is switched by switching a tail current of a differential transistor pair.

49. The signal transmission system as claimed in claim 48, wherein said tail current is switched by switching a current path between a route of said tail current of said transconductor and the other routes.

50. The signal transmission system as claimed in claim 49, wherein said current is switched by a transistor switch for switching the drain current of said differential transistor pair.

51. The signal transmission system as claimed in claim 47, wherein said current is switched by injecting to a source of the input transistor of said transconductor a current in such a direction as to turn off said input transistor.

52. The signal transmission system as claimed in claim 49, wherein said current is switched by use of a transistor connected in parallel such that the period during which said tail current flows is determined by the superposed portion of multi-phase clock signals.

53. The signal transmission system as claimed in claim 49, wherein said current is switched by use of a transistor connected in series such that the period during which said tail current flows is determined by the superposed portion of multi-phase clock signals.

54. The signal transmission system as claimed in claim 49, wherein a plurality of said sampling circuits sample different bit cells for a single determining circuit, and a weighted sum of the outputs of a plurality of said sampling circuits is determined.

55. A receiver circuit device comprising a

plurality of receiver units operating in interleaved fashion, wherein each receiver unit comprises:

a sampling circuit sampling an input signal;

a buffer circuit buffering an output of said sampling circuit;

a determining circuit determining an output of said buffer circuit; and

a buffer control circuit keeping a small input signal dependency of the output of said buffer circuit until carrying out said sampling.

56. The receiver circuit device as claimed in claim 55, wherein said buffer control circuit is a switch arranged between said buffer circuit and a power line.

57. The receiver circuit device as claimed in claim 55, wherein said buffer control circuit is a switch arranged between the output of said buffer circuit and a load device.

58. The receiver circuit device as claimed in claim 55, wherein said receiver unit further comprises a precharge circuit precharging an input of said determining circuit before said sampling circuit samples the input signal.

59. The receiver circuit device as claimed in claim 55, wherein said sampling circuit comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

60. The receiver circuit device as claimed in claim 55, wherein said buffer circuit comprises a plurality of buffer circuit units, and characteristics of a signal transmission path is compensated by adjusting a magnitude of an output of said buffer circuit units.

61. The receiver circuit device as claimed in claim 55, wherein said buffer circuit is a transconductor converting an input voltage to a current, and said buffer control circuit is a current source switch which keeps a

small current of said transconductor until carrying out said sampling.

62. The receiver circuit device as claimed in claim 55, wherein said buffer circuit comprises a micro current circuit for keeping a micro current flowing in said buffer circuit before said sampling circuit samples the input signal.

63. The receiver circuit device as claimed in claim 55, wherein said receiver unit further comprises a switching circuit, ensuring a substantially constant output of said buffer circuit when said sampling circuit samples the input signal, provided at the output of said buffer circuit.

64. A receiver circuit device comprising a plurality of receiver units operating in interleaved fashion, wherein each receiver unit comprises:

a sampling circuit sampling an input signal;

a buffer circuit buffering an output of said sampling circuit;

a determining circuit determining an output of said buffer circuit; and

a buffer control circuit keeping a substantially constant value of the output of said buffer circuit until carrying out said sampling.

65. The receiver circuit device as claimed in claim 64, wherein said buffer control circuit is a switch arranged between said buffer circuit and a power line.

66. The receiver circuit device as claimed in claim 64, wherein said buffer control circuit is a switch arranged between the output of said buffer circuit and a load device.

67. The receiver circuit device as claimed in claim 64, wherein said receiver unit further comprises a precharge circuit precharging an input of said determining circuit before said sampling circuit samples the input signal.

68. The receiver circuit device as claimed in claim 64, wherein said sampling circuit comprises a plurality of sample switches sampling a series of bits, and a plurality of said buffer circuits corresponding to said sample switches are provided.

69. The receiver circuit device as claimed in claim 64, wherein said buffer circuit comprises a plurality of buffer circuit units, and characteristics of a signal transmission path is compensated by adjusting a magnitude of an output of said buffer circuit units.

70. The receiver circuit device as claimed in claim 64, wherein said buffer circuit is a transconductor converting an input voltage to a current, and said buffer control circuit is a current source switch which keeps a small current of said transconductor until carrying out said sampling.

71. The receiver circuit device as claimed in claim 64, wherein said buffer circuit comprises a micro current circuit for keeping a micro current flowing in said buffer circuit before said sampling circuit samples the input signal.

72. The receiver circuit device as claimed in claim 64, wherein said receiver unit further comprises a switching circuit, ensuring a substantially constant output of said buffer circuit when said sampling circuit samples the input signal, provided at the output of said buffer circuit.

73. A receiver circuit device comprising a plurality of receiver units operating in interleaved fashion, wherein each receiver unit comprises:

a sampling circuit sampling an input signal;

a determining circuit determining an output of said sampling circuit; and

a sampling control circuit dynamically changing a transconductance from the input to the output of said sampling circuit and sufficiently reducing the

input signal dependency of the output of said sampling circuit at other than a sampling time point.

74. The receiver circuit device as claimed in claim 73, wherein said sampling control circuit changes by switching the transconductance from the input to the output of said sampling circuit.

75. The receiver circuit device as claimed in claim 74, wherein said transconductance is switched by switching a tail current of a differential transistor pair.

76. The receiver circuit device as claimed in claim 75, wherein said tail current is switched by switching a current path between a route of said tail current of said transconductor and the other routes.

77. The receiver circuit device as claimed in claim 76, wherein said current is switched by a transistor switch for switching the drain current of said differential transistor pair.

78. The receiver circuit device as claimed in claim 76, wherein said current is switched by injecting to a source of the input transistor of said transconductor a current in such a direction as to turn off said input transistor.

79. The receiver circuit device as claimed in claim 76, wherein said current is switched by use of a transistor connected in parallel such that the period during which said tail current flows is determined by the superposed portion of multi-phase clock signals.

80. The receiver circuit device as claimed in claim 76, wherein said current is switched by use of a transistor connected in series such that the period during which said tail current flows is determined by the superposed portion of multi-phase clock signals.

81. The receiver circuit device as claimed in claim 76, wherein a plurality of said sampling circuits sample different bit cells for a single determining circuit, and a weighted sum of the outputs of a plurality of said

sampling circuits is determined.